REMARKS/ARGUMENTS

Reconsideration and re-examination are hereby requested.

Claims 1 and 2 stand rejected under 35 U.S.C. 102(b) as being anticipated by Gaytan et al. (US 5,638,367).

Referring first to FIG. 4 of the subject patent application, it is noted that his system includes a multiplexer coupled to the accumulator register and the staging register. To put it in still another way, Applicant stores in sampling register 600, then FIRST SHIFTS in shifter 602, then sends the SHIFTED data to an accumulator 604 and staging register 606 with the SHIFTED data in the accumulator 604 being fed directly ***to one input*** of **a multiplexer** 608 and the SHIFTED data in the staging register 606 being fed to ***a second input*** of **the multiplexer** 608. Such an arrangement is not described in Gaytan et al. (US 5,638,367).

It is respectfully submitted that Gaytan et al. (US 5,638,367) does not feed data in an accumulator ***to one input*** of a multiplexer and a staging register feeding data to ***a second input*** of the multiplexer. It is respectfully requested that the examiner identify such a multiplexer in Gaytan et al.

Claim 1 points out that the multiplexer has W sections, each of the W sections being coupled to **a corresponding one of the W byte locations of the *accumulator register*** and a **corresponding one of the W byte locations of the *staging register***, each one of the sections coupling to an output thereof the byte location ***of the accumulator register or*** the byte location ***of the staging register*** selectively in accordance with the number of bytes in the prior gathered ones of the packets and the number of bytes being gathered from the currently gathered one of the packets to provide at an output of the multiplexer bytes to be transmitted as the transmitted block of data having the selected portions appended contiguously one to the other. ***Such an arrangement is not described in Gaytan et al.***

Claim 2 points out that the system includes a ***multiplexer*** having W sections, **each of the W sections being coupled to a corresponding one of the W byte locations of the *accumulator register*** and **a corresponding one of the W byte locations of *the staging***

register. each one of the sections coupling to an output thereof the byte location of the accumulator register or the byte location of the staging register selectively in accordance with the number of bytes in the prior distributed ones of the packets and the number of bytes being distributed from the currently distributed one of the packets to provide at an output of the multiplexer. ***Such an arrangement is not described in Gaytan et al.***

In the event a petition for extension of time is required by this paper and not otherwise provided, such petition is hereby made and authorization is provided herewith to charge deposit account No. 05-0889 for the cost of such extension.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 05-0889.

Respectfully submitted,

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Date

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